Inversion of hysteresis in quantum dot controlled quantum-wire transistor

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In a quantum-wire transistor, pronounced floating-gate function of quantum dots is demonstrated with large threshold hysteresis exceeding 1.5 V. The charge state of the quantum dots is electrically controlled and, by applying a critical bias voltage along the quantum wire, the charging mechanism of the quantum dots is deactivated or, for bias voltages above this critical bias point, even inverted. It is shown that the charging as well as discharging of the quantum dots can be selectively switched off; i.e., the floating-gate function of the quantum dots is suppressed. The inversion of the hysteresis is explained within the framework of a capacitor model and the control of the charging mechanism is attributed to a dynamic gate efficiency of the quantum wire, which can be either larger or smaller than the quantum dot gate efficiency.

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I. INTRODUCTION

A quantum wire (QW) positioned close to a quantum dot (QD) can serve as an efficient detector of the charge stored in this nearby QD.[1–13] The detector principle is based on the fact that the threshold voltage of the QW is shifted to more positive values the more electrons are stored in the QD. This operation is similar to the floating-gate function in quantum dot flash memories,[14] in which, due to the floating-gate operation of the QDs, the QW becomes locally depleted on the order of the single-electron-screening length.[15,16] For quantum dot flash memories, this floating-gate function of QDs has been demonstrated in several different material systems.[17–21]

In quantum dot flash memories, the charge state of the QDs can be controlled electrically as well as optically. It has been demonstrated that QDs can be charged or discharged optically with an electrical readout of the charge state[22,23] and also both electrical writing and erasing have been observed.[24,25] A very efficient way of controlling the QW has been obtained by positioning a QD in the constriction region of the QW,[16] i.e., in close vicinity to the maximum of the potential barrier. With increasing distance between QD position and barrier maximum, the electronic interplay between QD and QW is reduced and the floating-gate function decreases. Therefore, the QD-barrier-maximum distance is a control parameter for modulating the floating-gate function of the QDs. Indeed, for narrow QWs, the position of the potential barrier is strongly influenced by the drain voltage, an effect which is well known for short channels—the drain-induced barrier lowering.

In order to describe the floating-gate function of the QDs and the resulting threshold shift of the QW, it is necessary to consider the capacitive couplings in between the QW, the QDs, and the gate.[15,17,26–28] One approach to get experimental access to the capacitive couplings is based on the Coulomb-blockade oscillations. The floating-gate QDs create antidots in the QW and, in particular, coupled electron islands are formed. By transport spectroscopy, the capacitive couplings, e.g., between these electron islands and the gate, can be determined directly.[29–34]

Here, we report on a quantum-wire transistor (QWT) with embedded QDs operated as quantum dot flash memory. The device is based on a modulation-doped GaAs/AlGaAs heterostructure with embedded InGaAs QDs in close vicinity to the two-dimensional electron gas (2DEG). For the in-plane gated QWT, a common source configuration was used and the charge state of the QDs is controlled by the applied gate voltage. Large threshold hystereses of up to a value of 1.5 V are demonstrated in the linear as well as in the nonlinear transport regime. With increasing bias voltage, the charging mechanism of the QDs is modulated and, for a critical bias voltage, charging and discharging of the QDs are suppressed. For bias voltages beyond this critical point, an inversion of the charging mechanism is observed. By transport spectroscopy, the capacitive couplings between QDs, QW, and in-plane gates are analyzed and an analytic model is presented which allows explanation of the memory operation of the device. We attribute the inversion of the charging mechanism to a bias-voltage-induced shifting of the barrier maximum in the QW which comes along with a reduction in the gate efficiency. Due to this dynamic gate efficiency of the QW, which can be either larger or smaller than the QD-gate efficiency, the charging mechanism of the QDs is controlled by the bias voltage.

II. DEVICE FABRICATION

The device consists of a modulation-doped GaAs/AlGaAs heterostructure with self-assembled InGaAs QDs embedded in the center of an AlGaAs spacer. A schematic cross section of the layer sequence grown by molecular-beam epitaxy is shown in Fig. 1(a). Based on a semi-insulating GaAs substrate, a 200-nm-thick GaAs buffer followed by a superlattice was deposited. The superlattice consists of ten double layers of 25-nm-thick $Al_{0.2}Ga_{0.8}As$ and 10-nm-thick GaAs. On top of this, 2 μm GaAs and a 20-nm-thick $Al_{0.2}Ga_{0.8}As$ spacer were grown with InGaAs QDs in the center of the spacer. The heterostructure was completed by a 50-nm-thick Si-doped $Al_{0.2}Ga_{0.8}As$ layer with a Si concentration of 1×10^{18} cm^{-3} followed by a 10-nm-thick GaAs cap.

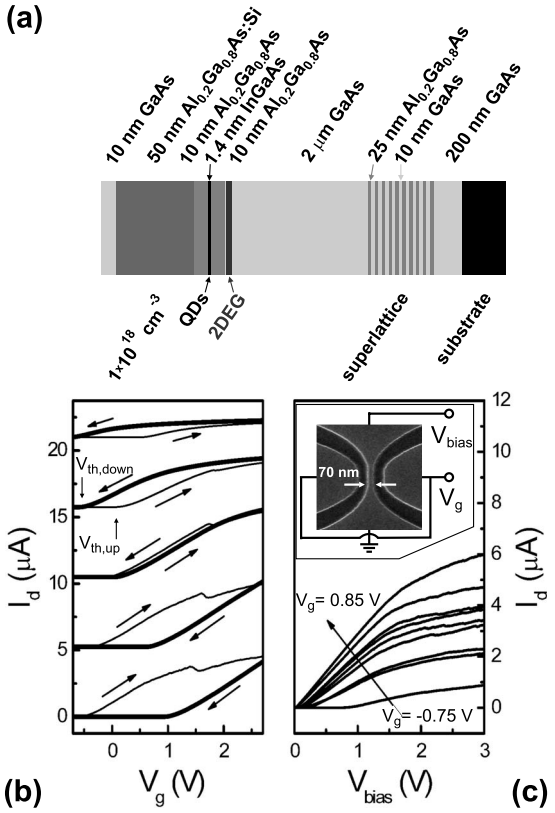

FIG. 1. (a) Schematic cross section of the layer sequence grown by molecular-beam epitaxy. (b) Transfer characteristics of the quantum-wire transistor for bias voltages $V_{\mathrm{bias}}=1.8$, 1.4, 1.0, 0.6, and 0.2 V (from down to top). The sweep directions of the gate voltage V_g are indicated by arrows. (c) Output characteristics of the quantum-wire transistor for gate voltages ranging from −0.75 to 0.85 V in steps of 0.2 V. Inset: scanning electron microscope (SEM) image of the quantum-wire transistor together with the electric setup.

At the heterostructure interface, a 2DEG is formed which resides approximately 80 nm below the sample surface. By depositing 1.4 nm InGaAs in the center of the spacer, self-assembled InGaAs QDs with a density of 5×10^{10} cm^{-2} and a diameter of 25 nm were formed due to Stranski-Krastanov growth mode. Both the density and the diameter of the QDs were obtained from a similar heterostructure in which the QDs were not overgrown (not shown here). The QDs were in close vicinity to the 2DEG and only separated by the lower, 10-nm-thick part of the $Al_{0.2}Ga_{0.8}As$ spacer from the 2DEG. Hence, the QDs can serve as floating gate on the 2DEG and, by adding electrons to the QDs, the 2DEG below the QDs is depleted due to the Coulomb repulsion of electrons.[19] Hall measurements performed at $T=4.2$ K provided an electron density of $n_{\mathrm{2DEG}}=4\times10^{11}$ cm^{-2} and an electron mobility of $\mu_e=8.5\times10^3$ cm^2/V s in the 2DEG, which are in good agreement with comparable heterostructures.[35,36] The InGaAs QDs deplete the nearby 2DEG and antidots are formed in the transport channel. These antidots act as additional scattering centers and reduce strongly the electron mobility.

Based on this heterostructure, an in-plane gated QWT (Refs. 37–39) with a 70-nm-wide constriction was fabricated by electron-beam lithography and wet-chemical etching. The gates and the QW were electrically separated by 90-nm-deep and 140-nm-wide etched trenches. The inset of Fig. 1(c) displays a SEM image of the device together with the electrical setup. A bias voltage V_{bias} was applied to the drain and a gate voltage V_g to the in-plane gates, whereas the source was grounded. All measurements were performed in the dark at 4.2 K.

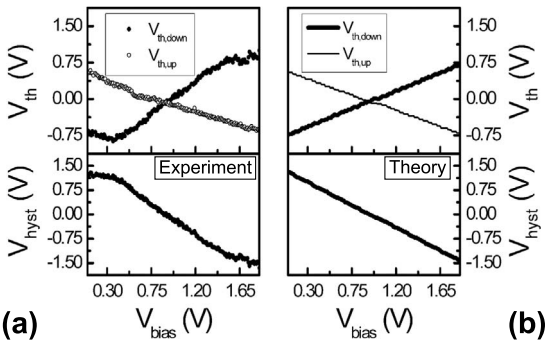

FIG. 2. (a) Upper part: threshold voltages $V_{\mathrm{th,up}}$ and $V_{\mathrm{th,down}}$ versus the bias voltage V_{bias}. Lower part: threshold hysteresis V_{hyst} versus V_{bias}. (b) Analytic modeling of $V_{\mathrm{th,up}}$, $V_{\mathrm{th,down}}$, and V_{hyst} versus V_{bias}.

III. DEVICE CHARACTERISTICS

Figure 1(b) shows the drain current versus the gate voltage for $V_{\mathrm{bias}}=1.8$, 1.4, 1.0, 0.6, and 0.2 V. The curves were offset by 5.25, 10.5, 15.75, and 21 μA for $V_{\mathrm{bias}}=1.4$, 1.0, 0.6, and 0.2 V, respectively. The sweep direction of V_g is indicated by arrows. In the up sweep of V_g, the QW is cut off for $V_g<-0.6$ V for $V_{\mathrm{bias}}=1.8$ V. With increasing gate voltage, the current increases, with a peak at $V_g=1.45$ V, and saturates for large gate voltages. In the down sweep of V_g, I_d decreases monotonically and the QW is cut off for $V_g<0.9$ V. A threshold hysteresis $V_{\mathrm{hyst}}=V_{\mathrm{th,up}}-V_{\mathrm{th,down}}=-1.5$ V, between the threshold voltages $V_{\mathrm{th,up}}$ and $V_{\mathrm{th,down}}$ of the up sweep and the down sweep of V_g, respectively, is observed. With decreasing V_{bias}, $V_{\mathrm{th,up}}$ shifts toward more positive gate voltages, whereas $V_{\mathrm{th,down}}$ decreases. Thus, the threshold hysteresis reduces and, for $V_{\mathrm{bias}}<1.0$ V, the sign of V_{hyst} is inverted.

For gate voltages varied from −0.75 to 0.85 V in steps of 0.2 V, the output characteristics of the QW are displayed in Fig. 1(c). With increasing V_{bias}, I_d increases linearly with a slope of 3 μA/V until $V_{\mathrm{bias}}=1.8$ V. Larger V_{bias} leads to a reduction in the slope and a maximum current of 6 μA is reached for $V_{\mathrm{bias}}=3$ V. With decreasing V_g, the maximum current and the slope are reduced. For gate voltages smaller than −0.75 V, the QW is cut off and, only for larger bias voltages does a current flow set in.

The upper part of Fig. 2(a) shows $V_{\mathrm{th,up}}$ and $V_{\mathrm{th,down}}$ versus V_{bias}. For low bias voltages, $V_{\mathrm{th,up}}$ is larger than $V_{\mathrm{th,down}}$. With increasing V_{bias}, $V_{\mathrm{th,up}}$ decreases and reaches a minimum value of −0.6 V for $V_{\mathrm{bias}}=1.8$ V. $V_{\mathrm{th,down}}$ increases with increasing V_{bias} and a maximum value of 0.9 V is observed for $V_{\mathrm{bias}}>1.6$ V. Interestingly, at a critical bias point $V_{\mathrm{bias}}=0.9$ V, $V_{\mathrm{th,up}}$ and $V_{\mathrm{th,down}}$ are identical and no threshold

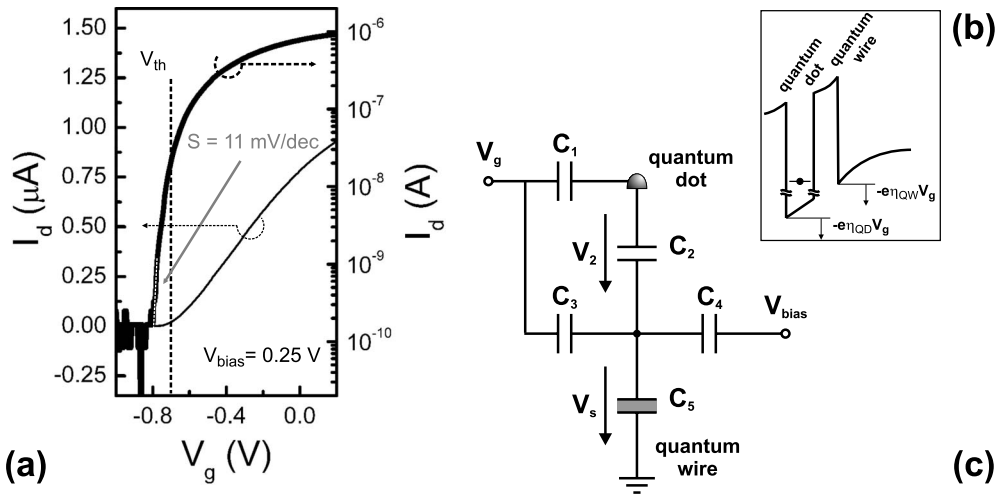

FIG. 3. (a) Drain current versus the gate voltage for $V_{bias}=0.25$ V. (b) Sketched conduction-band profile of a QD and the QW along the axis of growth. (c) Capacitive equivalent network of the device.

hysteresis occurs. For $V_{bias}>0.9$ V, the threshold hysteresis is inverted compared to the hysteresis for $V_{bias}<0.9$ V. The lower part of Fig. 2(a) displays V_{hyst} versus V_{bias}. For low bias voltages, V_{hyst} has a maximum value of 1.3 V and decreases with a slope of −2 V/V with increasing V_{bias}. At $V_{bias}=1.8$ V, a minimum threshold hysteresis of −1.5 V is reached.

We relate the observed threshold hysteresis in the transfer characteristics of the QW to a pronounced charging and discharging of the QDs in the spacer. Due to the floating-gate function of the QDs on the QW, stored electrons in the QD lead to an enhanced Coulomb repulsion on the electrons in the 2DEG and reduce the conductivity of the QW. As a result, the threshold voltage is shifted toward larger values of V_g the more electrons are stored in the QDs. According to the transfer characteristics, for high bias voltages, the QDs become charged for positive gate voltages, which is clearly indicated by the peaks found in the up sweep[40] [Fig. 1(b)] for $V_{bias}=1.8$, 1.4, and 1.0 V at $V_g=1.45$ V, and discharged for negative ones.

To explain the inversion of the hysteresis, we assume that the change in the electrostatic potentials of the QW and the QDs can vary significantly. Figure 3(b) shows schematically the conduction band of a QD and the QW along the axis of growth. Here, the highest occupied state of the QD is situated below the conduction-band minimum of the QW; i.e., the QD is charged. The in-plane gates couple capacitively to the QW and the QD and, thus, any change in the gate voltage results in a shift of the electrostatic potential of the QW and the QD. For small bias voltages, the potential along the QW is assumed to be symmetric. Therefore, the gates and the QW are situated in the same plane and the geometrical capacitance between the gates and the QW is larger compared to the geometrical capacitance between the gates and the QDs.[41] As a consequence, a gate-voltage change shifts the electrostatic potential of the QW more pronouncedly compared to the shift in the QD potential. A measure for this gate-induced potential shift are the gate efficiencies η_{QD} and η_{QW} of the QDs and the QW, respectively. For a given positive gate voltage, the change in electrostatic potential in the QW ($\propto -e\eta_{QW}V_g$) is larger than the change in the QDs ($\propto -e\eta_{QD}V_g$). For a sufficiently large increase in the gate voltage, the conduction-band minimum of the QW is lowered below the highest occupied state of the QD and the QD becomes discharged. On the other hand, for a given negative gate voltage, the electrostatic potentials of the QW and of the QDs increase and, for a critical gate voltage, electrons can tunnel from the QW into the QDs. This leads to a charging of the QDs which is self-limited due to the Coulomb blockade.[15]

IV. GATE EFFICIENCY

The gate efficiency η_{QW} of the QW can be determined from the subthreshold swing. In particular, the subthreshold swing S is defined as the gate-voltage sweep required to change the drain current by 1 decade and is given by $(k_BT/e)\ln 10$, with k_BT/e as the thermal voltage. Based on this formula, the minimum subthreshold swing is limited to 60 mV/decade at room temperature and to approximately 1 mV/decade in liquid helium. In a QW, in which η_{QW} is a measure of how a change in the electrochemical potential of the gates is transferred into a change in the electrostatic potential of the QW, η_{QW} can also be used to characterize the switching properties.[42] So η_{QW} is experimentally determined from the subthreshold swing S_{QW} of the QW with $\eta_{QW}=[(k_BT/e)\ln 10]S_{QW}^{-1}$.

For $V_{bias}=0.25$ V, Fig. 3(a) shows the drain current versus the gate voltage in both logarithmic and linear scales. In the subthreshold regime, i.e., for $V_g<-0.7$ V, a subthreshold swing of 11 mV/decade is found, which corresponds to $\eta_{QW}=9\%$. In Fig. 4(a), the gate efficiency η_{QW} of the QW is displayed versus V_{bias}. For small V_{bias}, a maximum value of 15% is observed and, with increasing V_{bias}, η_{QW} decreases with an average slope of −4%/V.

As discussed before, with increasing bias, the gate efficiency of the QW decreases, which can be related to a bias-induced shift of the potential barrier maximum in the QW. With increasing bias voltage, the barrier maximum shifts more and more toward the source contact. Therefore, the

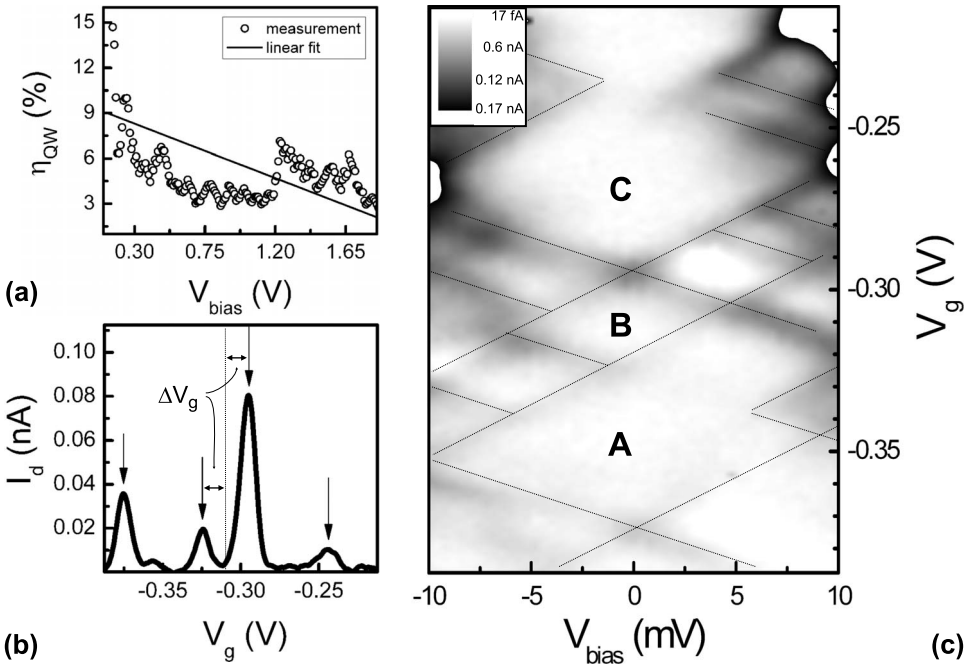

FIG. 4. (a) Gate efficiency of the QW versus V_{bias}. (b) Standard lock-in measurement of the drain current I_d versus the gate voltage V_g for $V_{bias}=0$. (c) Grayscale plot of the differential drain current as a function of the gate voltage for different bias voltages. Here, dark and bright regions correspond to currents above 0.17 nA and to currents below 17 fA, respectively.

effective distance between the gates and the barrier maximum increases and the gate efficiency η_{QW} is reduced. Such a dynamic shift cannot occur in the case of the QDs due to their three-dimensional confinement. Thus, the gate efficiency of the QDs is not affected by the bias voltage. At a critical bias point, i.e., for $\eta_{QD}=\eta_{QW}$, the electrostatic potentials in the QW and the QDs are changed equally with respect to the gate voltage and any electron charging or discharging is suppressed. A further increase in V_{bias} lowers η_{QW} below η_{QD} and the charging mechanism is inverted; i.e., now the QDs become charged for positive gate voltages and discharged for negative ones.

V. LINEAR TRANSPORT REGIME

We have also investigated the transport properties of the QW for small V_{bias} and determined the current-voltage characteristics by standard lock-in technique. Figure 4(b) shows the drain current I_d versus V_g for $V_{bias}=0$. Current peaks occur for $V_g=-0.375$, -0.325, -0.295, and -0.244 V as indicated by arrows. Interestingly, the peak positions are symmetric to the gate voltage $V_g=-0.31$ V (indicated by the dotted line) and equal shifts ΔV_g are observed with respect to this gate voltage. Figure 4(c) displays the differential drain current from $V_{bias}=-10$ mV to $V_{bias}=10$ mV. In this grayscale plot, dark regions correspond to currents above 0.17 nA and white ones correspond to currents below 17 fA. For higher bias voltages, adjacent peaks of high drain current converge with each other and diamondlike areas of low differential current are formed. For clarity, the borders of these areas are indicated by dotted lines. Three areas (A, B, and C) as well as isolated parallel structures can be identified.

We relate the observed peaks in the current-voltage characteristics to Coulomb-blockade oscillations which indicate the existence of laterally coupled electron islands in the 2DEG. The electron islands were formed due to the Coulomb repulsion between the charged QDs and the electrons in the 2DEG. For higher V_{bias}, Coulomb diamonds and resonance effects with drain and source were observed.[43] For a Coulomb diamond, the slope of its boundaries indicates the capacitive coupling between the electron island and the gate, the drain, and the source.[44] Together with a scaling factor, which is given by the ratio of the gate capacitance and the total capacitance of the electron island,[45] capacitances of 3.1, 5.6, and 3.1 aF between the electron islands and the in-plane gates were determined from the Coulomb diamonds A, B, and C, respectively. To estimate the size of the electron islands, the capacitance of each electron island is approximated by the capacitance of an isolated disk.[46] This leads to diameters of 16, 35, and 17 nm for the Coulomb diamonds A, B, and C, respectively. As one can easily see, the Coulomb diamonds A and C have almost identical characteristic values, whereas B differs significantly. Together with the observed symmetry of the peak position for zero bias, we conclude that two laterally coupled electron islands are formed in the 2DEG.[29,30] Thus, for the studied QW, a minimum number of three to four QDs in the spacer are necessary to form the electron islands.

VI. CAPACITOR MODEL

Based on these experimental results, the capacitive couplings are modeled by an equivalent network shown in Fig. 3(c). The gate voltage controls the QD via the capacitance C_1

as well as the QW, i.e., the potential barrier in the QW, via the capacitance C_3. The capacitances C_2 and C_4 describe the capacitive couplings of the QD and the port at which V_{bias} is applied, respectively, with the potential barrier. The switching voltage V_s is the voltage drop across the quantum capacitance C_5 in the QW, and is used to describe the conductivity of the device. Hence, V_s corresponds to the difference between the electrostatic potential and the electrochemical potential in the QW and characterizes, e.g., the cutoff condition or the gate efficiency of the QW.[47,48] Solving this capacitive network leads to

$$\left[C_2^2 - (C_1 + C_2)\sum_{i=2}^{5} C_i\right] V_s = -neC_2 + (C_1 + C_2)C_4 V_{\text{bias}} + \frac{1}{2}\left[\sum_{j=1}^{3}\sum_{k=1}^{3}\left(C_j C_k - \frac{1}{3}C_j^2\right)\right] V_g, \tag{1}$$

with e as the electron charge and n as the number of electrons in the QD. For $V_s=0$, no electrons are in the QW and the QW is cut off. For this case, the threshold voltage V_{th} is given by

$$V_{\text{th}} = \frac{1}{\frac{1}{2}\sum_{j=1}^{3}\sum_{k=1}^{3}\left(C_j C_k - \frac{1}{3}C_j^2\right)}\left[neC_2 - V_{\text{bias}}(C_1 + C_2)C_4\right]. \tag{2}$$

According to Eq. (2), V_{th} depends on the number of electrons in the QD. Furthermore, V_{th} shifts linearly toward negative values with increasing bias voltage. In our device, the QDs are charged due to electron tunneling from the QW, i.e., via C_2. Modeling of comparable systems showed that n is determined by

$$n = \frac{eV_2}{E_c}, \tag{3}$$

with E_c as the charging energy of the QD and V_2 as the voltage drop across C_2.[46,49] V_2 is the difference between the electrostatic potentials of the QW and the QD and can be written as $V_2 = V_g(\eta_{\text{QD}} - \eta_{\text{QW}})$. For self-assembled QDs, the single-particle energy-level spacing is generally larger than the Coulomb energy and cannot be neglected.[50] Based on calculations of the electronic structure of self-assembled InGaAs QDs on a GaAs layer, the single-particle energy-level spacing was simulated and the charging energy can be estimated as $E_c=30$ meV.[51] The bias dependency of η_{QW} was approximated by the linear fit shown in Fig. 4(a). For η_{QD}, a constant value of 5% was assumed, which is equal to η_{QW} at the critical bias point, i.e., $V_{\text{bias}}=0.9$ V. The capacitance C_3 was set to 3.1 aF, which follows directly from the extracted values in the linear transport regime. Based on the gate efficiencies η_{QW} and η_{QD} for small bias voltages, $C_1 = C_3/2$ was concluded. According to Eq. (2), the threshold voltages $V_{\text{th,up}}$ and $V_{\text{th,down}}$ were modeled with $C_2=7$ aF and $C_4=0.5$ aF, and are shown in Fig. 2(b). If we assume that only four QDs serve as floating gate, the maximum change in the charge state within one gate sweep cycle is limited to about ten electrons per QD.

VII. SUMMARY

In summary, we have demonstrated pronounced floating-gate function of QDs in a quantum dot flash memory with large threshold hysteresis exceeding 1.5 V. With increasing bias voltage, the barrier maximum in the QW is shifted toward source and the gate efficiency of the QW is reduced. Due to this dynamic gate efficiency of the QW, the floating-gate function of the QDs is controlled by the bias voltage and the charging mechanism of the QDs is inverted for large bias voltages. By transport spectroscopy, the capacitive couplings between QDs, QW, and in-plane gates are analyzed and, in the frame of a capacitor model, the threshold voltages and the threshold hysteresis were calculated. It is concluded that the observed threshold hysteresis is attributed to a maximum number of up to ten electrons per QD.

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